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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,171	09/19/2003	Rodney E. Hooker	CNTR.2213	6328

23669 7590 01/11/2007
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EXAMINER	
PATEL, HETUL B	
ART UNIT	**PAPER NUMBER**
2186	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	01/11/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 01/11/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PTO@HUFFMANLAW.NET

Office Action Summary	Application No.	Applicant(s)	
	10/665,171	HOOKER, RODNEY E.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,15,16,32-40 and 46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,9 and 32* is/are rejected.

7)☒ Claim(s) *2,5-8,15,16,33-40 and 46* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on December 18, 2006 has been entered and carefully considered.

2. Claims 10-14 and 41-45 are cancelled; and claims 1-5, 7-9, 15-16, 32-36, 38-40 and 46 are amended. Therefore, claims 1-9, 15-16, 32-40 and 46 are currently pending in this application.

3. Applicant's arguments filed on December 18, 2006 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 46 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 46 recites the limitation "the second one of the plurality of part-page ownership bits" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim. It appears that this claim should be depend upon claim 36 instead of claim 35.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3-4, 9 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kyker et al. (USPN: 6,594,734) hereinafter, Kyker.

As per claim 1, Kyker teaches an apparatus in a pipeline microprocessor (i.e. 301A in Fig. 4A), for ensuring coherency of instructions within stages of the pipeline microprocessor, the apparatus comprising: instruction cache management logic (i.e. 415 in Fig. 4A), configured to receive an address corresponding to a next instruction to be fetched (i.e. the physical address received by the ITLB), and configured to detect that a part of a memory page corresponding to said next instruction cannot be freely accessed without checking for coherency of the instructions within said part of said memory page (i.e. the physical addresses stored in ITLB) and, upon detection, configured to provide said address; and synchronization logic, configured to receive said address from said instruction cache management logic, and configured to direct

data cache management logic to check for coherency of the instructions within said part of said memory page, and, if the instructions are not coherent within said part of said memory page, said synchronization logic is configured to direct the pipeline microprocessor to stall a fetch of said next instruction until the stages of the pipeline microprocessor have executed all preceding instructions (e.g. see the abstract, claim 17 and Fig. 4A). Kyker further discloses that when a snoop is triggered, the physical address of the store into memory is provided to the snoop port and the ITLB performs a comparison with all the physical page addresses located within the ITLB 412 to determine whether a store into memory has addressed a page which may be stored in the instruction cache 414A. If a match is found, a store occurred into memory within a page of instructions that may be stored within an instruction cache and the cache and the instruction pipeline may be incoherent with memory (e.g. see Col. 7, lines 6-15). In other words, Kyker does teach that the instruction cache management logic evaluates an instruction translation lookaside buffer (ITLB) entry corresponding to the address of the next instruction to detect that said part cannot be freely accessed, as claimed.

Although Kyker does not specifically disclose that the data cache management logic evaluates a DTLB entry corresponding to the address to detect that the instructions are not coherent within said part of the memory page, Kyker does teach, in Col. 7, lines 6-15, about evaluating ITLB entry corresponding to the address to detect that the instruction is not coherent within the part of the memory page. Kyker also discloses that "[T]he present invention has been described herein with reference to instructions in an instruction translation lookaside buffer (ITLB) and an instruction

cache, but it is equally applicable for cache coherency between memory and a cache storing data where a translation lookaside buffer is used" (e.g. see Col. 14, lines 16+). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to also evaluate a DTLB entry corresponding to the address of the next instruction to detect that the instructions are not coherent within said part of the memory page. In doing so, the data coherency within the part of the memory page can be detected.

As per claim 32, Kyker teaches a method in a pipeline microprocessor (i.e. 301 in Fig. 4A), for ensuring coherency of instructions within stages of the pipeline microprocessor, the apparatus comprising: within instruction cache (i.e. 414A in Fig. 4A), detecting that a part of a memory page corresponding to a next instruction to be fetched cannot be freely accessed without checking for coherency of the instructions within the part of the memory page; directing logic within a data cache to check for coherency of the instructions within the part of the memory page; and if the instructions are not coherent, stalling a fetch of the next instruction from the instruction cache until the stages of the pipeline microprocessor have executed all preceding instructions (e.g. see the abstract, claim 17 and Fig. 4A). Kyker further discloses that when a snoop is triggered, the physical address of the store into memory is provided to the snoop port and the ITLB performs a comparison with all the physical page addresses located within the ITLB 412 to determine whether a store into memory has addressed a page which may be stored in the instruction cache 414A. If a match is found, a store occurred into memory within a page of instructions that may be stored within an instruction cache and

the cache and the instruction pipeline may be incoherent with memory (e.g. see Col. 7, lines 6-15). In other words, Kyker does teach that the instruction cache management logic evaluates an instruction translation lookaside buffer (ITLB) entry corresponding to the address of the next instruction to detect that said part cannot be freely accessed, as claimed.

Although Kyker does not specifically disclose that the data cache management logic evaluates a DTLB entry corresponding to the address to detect that the instructions are not coherent within said part of the memory page, Kyker does teach, in Col. 7, lines 6-15, about evaluating ITLB entry corresponding to the address to detect that the instruction is not coherent within the part of the memory page. Kyker also discloses that "[T]he present invention has been described herein with reference to instructions in an instruction translation lookaside buffer (ITLB) and an instruction cache, but it is equally applicable for cache coherency between memory and a cache storing data where a translation lookaside buffer is used" (e.g. see Col. 14, lines 16+). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to also evaluate a DTLB entry corresponding to the address of the next instruction to detect that the instructions are not coherent within said part of the memory page. In doing so, the data coherency within the part of the memory page can be detected.

As per claim 3, Kyker teaches the claimed invention as described above and furthermore, Kyker teaches that the ITLB entry corresponds to the memory page (e.g. see claim 17); and as per Col. 14, lines 16+, "[T]he present invention has been

described herein with reference to instructions in an instruction translation lookaside buffer (ITLB) and an instruction cache, but it is equally applicable for cache coherency between memory and a cache storing data where a translation lookaside buffer is used", therefore, once the DTLB is implemented as referred above, the DTLB entry also corresponds to the memory page.

As per claim 4, Kyker teaches the claimed invention as described above and furthermore, Kyker teaches that the ITLB entry comprises a plurality of part-page ownership bits (i.e. FINE HITS bits) (e.g. see Col. 11, line 59+); and as per Col. 14, lines 16+, "[T]he present invention has been described herein with reference to instructions in an instruction translation lookaside buffer (ITLB) and an instruction cache, but it is equally applicable for cache coherency between memory and a cache storing data where a translation lookaside buffer is used", therefore, once the DTLB is implemented as referred above, the DTLB entry also comprise a plurality of part-page ownership bits.

As per claim 9, Kyker teaches the claimed invention as described above and furthermore, Kyker teaches that the plurality of part-page ownership bits comprise four part-page ownership bits in the ITLB entry, and wherein said part comprises one-quarter of said memory page (i.e. "[T]he FINE HIT bits for simplicity are selected in the preferred embodiment to provide a granularity of 1K or 1024 addresses within a 4K page of memory. While this is the size utilized in the preferred embodiment, other granularities may be utilized. In the preferred embodiment, the ITLB 412 includes four FINE HIT bits with each line of translation contained therein, each being associated with a 1K block of addresses within a 4K page. ") (e.g. see Col. 11, line 59+). As per Col.

14, lines 16+, "[T]he present invention has been described herein with reference to instructions in an instruction translation lookaside buffer (ITLB) and an instruction cache, but it is equally applicable for cache coherency between memory and a cache storing data where a translation lookaside buffer is used", therefore, once the DTLB is implemented as referred above, each of the DTLB entry also comprise four part-page ownership bits, as claimed.

Allowable Subject Matter

6. Claims 2, 5, 33 and 36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 6-8, 15-16, 34-35, 37-40 and 46 would also be allowable as they further limit the objected claims 5, 33 and 36.

Remarks

7. As to the remark, Applicant asserted Kyker does not teach a technique that employs both an ITLB and a DTLB each having entries that correspond to an address for a next instruction.

Examiner respectfully traverses Applicant's remark for the following reasons:

First of all, Examiner would like to point out to Applicant that none of the pending claims recite/include either an ITLB or a DTLB. All claims refer to only the ITLB entry and the DTLB entry.

Although Kyker does not specifically disclose about an ITLB and a DTLB each having entries that correspond to an address for a next instruction, Kyker does teach an ITLB having entries that correspond to an address for a next instruction (e.g. see claim 17). As per Col. 14, lines 16+, Kyker also disclose that "[T]he present invention has been described herein with reference to instructions in an instruction translation lookaside buffer (ITLB) and an instruction cache, but it is equally applicable for cache coherency between memory and a cache storing data where a translation lookaside buffer is used", therefore, once the DTLB is implemented as referred above, each of the DTLB entry also correspond to the address of the next instruction, as claimed.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

H B Patel 01/04/2007
Hetul Patel
Patent Examiner
Art Unit 2186